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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

MW

Office Action Summary	Application No.	Applicant(s)	
	10/043,474	BARAZ ET AL.	
	Examiner	Art Unit	
	Chih-Ching Chow	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8,10,12-17,19 and 21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8,10,12-17,19 and 21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to amendment dated August 9, 2007.

2. Per Applicants' request, claims 1, 3, 4, 5, 6, 10, 12, 13, 14, 15, 19, 21, 22, 23, and 24 have been amended. Claims 2, 9, 11, 18, 20 and 27 have been canceled.

3. Claims 1, 3-8, 10, 12-17, 19, 21-26 remain pending.

Response to Amendment

4. Applicants' amendment filed on 11/8/07, responding to the 8/9/07 Office action provided in the 35 USC § 102 and 103 rejections for claims 1-8, 10-17, 19-26. The examiner has reviewed the amended claims 1, 3, 4, 5, 6, 10, 12, 13, 14, 15, 19, 21, 22, 23, and 24 respectfully. The amendment has brought up 35 USC § 112 rejections, see below.

Response to Arguments

5. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection necessitated by Applicant's amendments to the claims.

Claim Rejections - 35 USC § 112

6. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 recites: "A machine-implemented method comprising: analyzing one or more instructions of a first program; and modifying the first program to expand a register set that includes a

first set of local registers and a second set of output registers for a routine in the first program transparently to execution of the first program that includes adding one or more registers to the register set between the first set and the second set to generate an expanded register set, wherein the one or more registers of the expanded register set are used by a second program to store data used to analyze the execution of the first program; *identifying one or more register moves that move data between registers of the expanded register set* for the routine, and modifying the first program to form the identified one or more register move." – the amended claim (under lined part) indicates that the expanded register set is the additional registers (38-42 in FIG. 3, item 301), however the 'move data between registers of the expanded register set for the routine' is not clearly defined; the related description in paragraphs [33]-[41] do not explain moving data in between the additional registers, from FIG. 3, the data moving is not between registers 38-42 (see item 302); the moving is not 'between the registers of the expanded register set', the amended claim 1 fails to match what was illustrated in FIG. 3. Further the amended claim 1 recites '*move data between registers of the expanded register set*', there is no data move in between the expanded registers (registers 38-42), the connections between the modifying the first program and the moving of data between the registers of the expanded register set is not clear. Claim 1 does not particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claims 3-8 depend on claim 1, they are rejected under 35 USC § 112 (2) for the same reason.

8. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter

which applicant regards as the invention. Claim 10 recites: "A machine-readable medium having instructions that, if executed by a machine, cause the machine to perform a method comprising: analyzing one or more instructions of a first program; modifying the first program to expand a register set that includes a first set of local registers and a second set of output registers for a routine in the first program transparently to execution of the first program that includes adding one or more registers to the register set between the first set and the second set to generate an expanded register set, wherein the one or more registers of the expanded register set are used by a second program to store data used to analyze the execution of the first program; identifying one or more register moves that move data between registers of the expanded register set for the routine; and modifying the first program to perform the identified one or more resister moves." – the amended claim (under lined part) indicates that the expanded register set is the additional registers (38-42 in FIG. 3, item 301), however the 'move data between registers of the expanded register set for the routine' is not clearly defined; the related description in paragraphs [33]-[41] do not explain moving data in between the additional registers, from FIG. 3, the data moving is not between registers 38-42 (see item 302); the moving is not 'between the registers of the expanded register set', the amended claim 10 fails to match what was illustrated in FIG. 3. Further, the amended claim 10 recites '*move data between registers of the expanded register set*', there is no data move in between the expanded registers (registers 38-42), the connections between the modifying the first program and the moving of data between the registers of the expanded register set is not clear. Claim 10 does not particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claims 12-17 depend on claim 10, they are rejected under 35 USC § 112 (2) for the same reason.

10. Claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 19 recites: "A system comprising: a processor to execute instructions; a medium having instructions to analyze one or more of a first program and to modify the first program to expand a register set that includes a first set of local registers and a second set of output registers for a routine in the first program transparently to execution of the first program that includes adding one or more registers to the register set between the first set and the second set to generate an expanded register set, wherein the one or more registers of the expanded register set are used by a second program to store data used to analyze the execution of the first program, wherein the medium has instructions to identify one or more register moves that move data between registers of the expanded register set for the routine; and modifying the first program to perform the identified one or more resister moves." – the amended claim (under lined part) indicates that the expanded register set is the additional registers (38-42 in FIG. 3, item 301), however the 'move data between registers of the expanded register set for the routine' is not clearly defined; the related description in paragraphs [33]-[41] do not explain moving data in between the additional registers, from FIG. 3, the data moving is not between registers 38-42 (see item 302); the moving is not 'between the registers of the expanded register set', the amended claim 19 fails to match what was illustrated in FIG. 3. Further the amended claim 19 recites '*move data between registers of the expanded register set*', there is no data move in between the expanded registers (registers 38-

42), the connections between the modifying the first program and the moving of data between the registers of the expanded register set is not clear. Claim 19 does not particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claims 21-26 depend on claim 19, they are rejected under 35 USC § 112 (2) for the same reason.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1, 4-8, 10, 13-17, 19, 22-26 are rejected under are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,926,646 by Pickett et al., hereinafter "Pickett", in view of U.S. Patent No. 5, 875,318 by Langford (hereinafter "Langford").

CLAIM	Pickett / Langford
1. A machine-implemented method comprising: analyzing one or more instructions of a first program; ~~and~~ modifying the first program to expand a register set <u>that includes a first set of local registers and a second set of output registers</u> for a routine in the first program transparently to execution of the first program that includes adding one or more registers to the register set	Pickett teaches the feature of expanding a register set. See Pickett's Abstract "A microprocessor includes **an expanded set of registers** in addition to the architected set of registers specified by the microprocessor architecture employed by the microprocessor. The **expanded set of registers are memory-mapped within the context of the program being executed**. (*expanding a*

between the first set and the second set to generate an expanded register set, wherein the one or more registers of the expanded register set are used by a second program to store data used to analyze the execution of the first program; *identifying one or more register moves that move data between registers of the expanded register set* for the routine, and modifying the first program to form the identified one or more register move.

register set)", and further "The implemented portion of the **expanded registers** are accessed as register accesses, while the unimplemented portion are converted to memory accesses. The **decode unit within the microprocessor may be configured to convert instructions** which are coded to access the unimplemented **expanded registers into memory operations to access the corresponding memory location**." --*the decoding process is considered as analyzing one or more instructions of a program*. Pickett teaches all aspects of claim 1, but he does not mention 'adding one or more registers to the register set between the first set and the second set to generate an expanded register set' specifically, however, Langford teaches it in an analogous prior art. In Langford's column 3, lines 1-33, "Source code 10 is made of a sequence of instructions which comprise instruction 12 and instruction (m). Instruction 12 modifies instruction (m). This modification may be in the form of **incrementing** or **using a different register to store a particular data each time the code is executed**. For example, the basic instruction of instruction (m) may be to **copy the contents of a register into memory using another register** and an offset to form the address of the memory store such as: copy Cx Dsi, where Cx is the register from which the data will be copied, **Ds is the register**

containing the base address of the data and (i) is an offset to Ds Instruction 12 may be incrementing the offset (i). Therefore each time the code is executed, the **content of register Cx is copied into a different memory location.**" – adding register(s) staring from base address Cx, moving the data when executing the code. For 'modifying first program' feature see Pickett's column 2, lines 56-60, "An application program **may make use of the expanded registers** by assigning the most-often used operands in the program to the set of memory locations corresponding to the expanded registers. The application programmer may than **code instructions which access these operands** with **register identifiers corresponding to the expanded** registers." And column 2, lines 43-55, "The microprocessor includes an **expanded set of registers** in addition to the architected set of registers specified by the microprocessor architecture employed by the microprocessor. **The expanded set of registers are memory-mapped within the context of the program being executed**. **Upon a context switch**, the microprocessor **saves the state of the expanded registers to the corresponding memory locations**. Advantageously, the context save area defined by the microprocessor architecture is not modified by adding the provided registers. Additionally, since the

microprocessor manages the **save and restore of the expanded registers upon context switches**, the addition of the expanded registers is **transparent to operating system software**".– *modifying the program and transparently to execution of the program.* For using expanded registers by a second program feature see Pickett's column 2, lines 25-28, "As used herein, **a context switch** is an event in which one context, corresponding to a **first program, is replaced within the microprocessor by another context corresponding to a second program**". Further see Pickett's Abstract, "The application programmer may than code instructions which access these operands with **register identifiers corresponding to the expanded registers**. (*identifying one or more registers*)." See claim rejection 1 has for 'modifying program' feature.
It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to supplement Pickett's disclosures of the analyzing program by expanding registers taught by Langford, for the purpose of adjusting the appropriate size of registers for target code to be comparable to the execution of the source code (Langford column 3, lines 15-34).

4. The method of claim 1, wherein the modifying the first program comprises

Claim 1 rejection is incorporated. Further, see Pickett's column 17, lines

modifying the first program to expand a the register set for a callee routine of the first program.

19-29, "An additional consideration in the use of instruction redefinition by the application program is the use of operating system routines by the application program. It is desirable to allow instruction redefinition to be utilized by the application program, but to disable instruction redefinition when the operation system executes. In this manner, microprocessor 10 may employ instruction redefinition without requiring the operating system to be rewritten. Particularly, if privileged instructions are selected as redefinable instructions, the operating system may need to execute the privileged instruction within the **called operating system routine.**" And column 17 lines 30-34, "Disabling instruction redefinition mode upon context switches effects the disablement of instruction redefinition mode when the operating system begins executing via a context switch. However, **application programs often call operating system service routines**." – the operating system routine is considered as a callee routine, to expand a register for a callee routine of the first program.

5. The method of claim 4, comprising: modifying the first program to expand a the register set for a caller routine that is to call the callee routine.

Claim 4 rejection is incorporated. See Pickett's disclosure cited in claim 4 rejection, it covers both callee routine and caller routine, and the caller routine can call the callee routine.

6. The method of claim 5, wherein the

Claim 5 rejection is incorporated ,

modifying the first program to expand ~~a~~ the register set for the callee routine comprises modifying the first program to expand a register set that includes the one or more registers of the register set for the caller routine.	further see claim 4 rejection.
7. The method of claim 5, comprising: (a) identifying one or more register moves for the register set of the caller routine; and (b) modifying the first program to perform the identified one or more register moves prior to or upon returning from the callee routine to the caller routine.	Claim 5 rejection is incorporated , further see claim 1 rejection.
8. The method of claim 5, comprising: (a) identifying a register move from a register added to the register set for the caller routine to a register added to the register set for the callee routine; and (b) modifying the first program to perform the identified register move.	Claim 5 rejection is incorporated , further see claim 1 rejection.
10. A machine-readable medium having instructions that, if executed by a machine, cause the machine to perform a method comprising: analyzing one or more instructions of a first program; and modifying the first program to expand a register set that includes a first set of local registers and a second set of output registers for a routine in the first program transparently to execution of	Pickett's teaching also covers a machine-readable medium having instructions, see Pickett's claim 33. Claim 10 is a machine-readable version of claim 1, therefore see claim 1 rejection.

the first program that includes adding one or more registers to the register set between the first set and the second set to generate an expanded register set, wherein the one or more registers of expand ~~an~~ the expanded register set are used by a second program to store data used to analyze the execution of the first program;

identifying one or more register moves that move data between registers of the expanded register set for the routine; and

modifying the first program to perform the identified one or more register moves.

13. The machine-readable medium of claim 10, wherein the modifying the first program comprises modifying the first program to expand ~~a~~ the register set for a callee routine of the first program.

Claim 10 rejection is incorporated , further see claim 4 rejection.

14. The machine-readable medium of claim 13, wherein the method comprises:
modifying the first program to expand ~~a~~ the register set for a caller routine that is to call the callee routine.

Claim 13 rejection is incorporated , further see claim 5 rejection.

15. The machine-readable medium of claim 14, wherein the modifying the first program to expand ~~a~~ the register set for the callee routine comprises modifying the first program to expand ~~a~~

Claim 14 rejection is incorporated , further see claim 6 rejection.

the register set that includes one or more registers of the register set for the caller routine.

16. The machine-readable medium of claim 14, wherein the method comprises:
(a) identifying one or more register moves for the register set of the caller routine; and

(b) modifying the first program to perform the identified one or more register moves prior to or upon returning from the callee routine to the caller routine.

For the feature of claim 14 see claim 14 rejection. For the rest of the claim 16 feature see claim 7 rejection.

17. The machine-readable medium of claim 14, wherein the method comprises:
(a) identifying a register move from a register added to the register set for the caller routine to a register added to the register set for the callee routine; and

(b) modifying the first program to perform the identified register move.

Claim 14 rejection is incorporated , further see claim 8 rejection.

19. A system comprising:

a processor to execute instructions; ~~and~~ a medium having instructions to analyze one or more of a first program and to modify the first program to expand a register set that includes a first set of local registers and a second set of output registers for a routine in the first program transparently to execution of

Claim 19 is a system version of claim 1, therefore see claim 1 rejection.

the first program that includes adding one or more registers to the register set between the first set and the second set to generate an expanded register set, wherein the one or more registers of the expanded register set are used by a second program to store data used to analyze the execution of the first program; wherein the medium has instructions to identify one or more register moves that move data between registers of the expanded register set for the routine; and modifying the first program to perform the identified one or more resister moves.

22. The system of claim 19, the medium having instructions to modify the first program to expand ~~a~~ the register set for a callee routine of the first program.

Claim19 rejection is incorporated , further see claim 4 rejection.

23. The system of claim 22, the medium having instructions to modify the first program to expand ~~a~~ the register set for a caller routine that is to call the callee routine.

For the feature of claim 22 see claim 22 rejection. For the rest of the features see claim 5 rejection.

24. The system of claim 23, the medium having instructions to modify the first program to expand ~~a~~ the register set that includes one or more registers of the register set for the caller routine.

For the feature of claim 23 see claim 23 rejection. For the rest of the features see claim 6 rejection.

25. The system of claim 23, the medium having instructions to identify one or more register moves for the register set of the caller routine and to modify the

For the feature of claim 23 see claim 23 rejection. For the rest of the features see claim 7 rejection.

first program to perform the identified one or more register moves prior to or upon returning from the callee routine.	
26. The system of claim 23, the medium having instructions to identify a register move from a register added to the register set for the caller routine to a register added to the register set for the callee routine and to modify the first program to perform the identified register move.	For the feature of claim 23 see claim 23 rejection. For the rest of the features see claim 8 rejection.

14. Claims 3, 12, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,926,646 by Pickett et al., (hereinafter "Pickett"), in view of U.S. Patent No. 5, 875,318 by Langford (hereinafter "Langford"), further in view of U.S. Patent No. 5, 644,709 by Todd Michael Austin (hereinafter "Austin").

CLAIM	**Pickett /Longford /Austin**
3. The method of claim ~~2~~ 1, wherein the identifying comprises: (a) defining one or more move chains for the expanded register set, and (b) identifying a sequence of one or more register moves based on the defined one or more move chains.	For the feature of claim 1 see claim 1 rejection. Pickett teaches all aspects of claim 3, but he does not mention 'move chain' specifically, however, Austin teaches it in an analogous prior art. In Austin column 7, lines 19-26, "A **call-chain** is the state of the stack at some point in a program's execution; it is composed of **a sequence of function names**; functions higher in the **call-chain** call (possibly indirectly) the functions lower in the call **chain**; neighbors in the **call-chain** share a

direct **caller-callee relationship**. A partial **call-chain** is a subset of the current complete call-chain, usually taken from the bottom of the complete call chain; partial call-chains are usually employed to reduce storage requirements."
It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to supplement Pickett's and Longford's disclosures of the analyzing program and expanding registers by call chain taught by Austin, for the purpose of adjusting the appropriate counts at calls (Austin column 7, lines 34-35) thus no callee routine would be left out during a program rearrangement.

12. The machine-readable medium of claim ~~11~~ 10, wherein the identifying comprises:
(a) defining one or more move chains for the expanded register set, and
(b) identifying a sequence of one or more register moves based on the defined one or more move chains.

Claim 10 rejection is incorporated , further see claim 3 rejection.

21. The system of claim ~~20~~ 19, the medium having instructions to define one or more move chains for the expanded register set and to identify a sequence of one or more register moves based on the defined one or more move chains.

Claim 19 rejection is incorporated , further see claim 3 rejection.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sevcik, US Patent No. 3,931,505, discloses a program controlled data processing system which includes two data manipulation units generally operated in parallel. The two data manipulation units, however, by design react differently in the execution of certain program order words. The system includes a circuit arrangement which compares data generated by the two data manipulation units and generates comparison signals indicating the identity or lack of identity of the compared data.

Ziegler, US Patent No. 6,925,535, discloses method and apparatus for conditioning program control flow on the presence of requested data in a cache memory. In a data processing system that includes a cache memory and a system memory coupled to a processor, in various embodiments program control flow is conditionally changed based on whether the data referenced in an instruction are present in the cache memory. When an instruction that includes a data reference and an alternate control path is executed, the control flow of the program is changed in accordance with the alternate control path if the referenced data are not present in the cache memory.

Batcher, US Patent No. 5,668,947, discloses a method and apparatus for testing a digital integrated circuit (IC) for faults wherein the IC includes a memory, a microprocessor, an operand register, and a random data generator which is responsive to integrated circuit data indicative of the instantaneous IC state. A short test code including operational code instructions in the memory is performed by the microprocessor which manipulates data in the operand register.

Periodically, the random data generator provides seed data to the microprocessor which changes the test code in a random manner and modifies the data stored in the operand register.

Mitsuishi et al., US Patent No. 5,666,510, discloses a CPU has an upper compatibility with a low-order CPU to expand a continuously usable address space relatively. For latching data information, registers are constructed for being an address register with a bit number larger than the address bit number of a low-order CPU. The data information has its byte/word size specified by the size bit of an operation code. The utilization of the data information of a long word size is specified by either the prefix code or the operation code to which is newly added the same bit number as that of the low-order CPU. For the data information of the byte size, the high-/low-orders of the byte size register to be utilized are specified by predetermined 1 bit of a register specifying field.

Arora et al., US Patent No. 6,119,218, discloses a method and apparatus for prefetching data in a computer system that includes a processor. A prefetch instruction is executed and, in response, data is prefetched from a memory location. It is determined if a memory exception occurred during the prefetching of the data. If a memory exception occurred, the exception is handled if the prefetch instruction indicates to do so.

16. The following summarizes the status of the claims:

35 USC § 112 rejection: Claims 1, 3-8, 10, 12-17, 19, 21-26

35 USC § 103 rejection: Claims 1, 3-8, 10, 12-17, 19, 21-26

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chih-Ching Chow whose telephone number is 571-272-3693. The examiner can normally be reached on 7:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen can be reached on 571-272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature of relating to the status of this application should be directed to the **TC2100 Group receptionist: 571-272-2100**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chih-Ching Chow
Examiner
Art Unit 2191
January 11, 2008

CC

MARY STEELMAN
PRIMARY EXAMINER